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Amdt. dated 11/12/2003
Reply to Office Action of September 5, 2003

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Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1   1.   (Currently Amended) A processor chip, comprising:

2   a processing core; and

3   at least one bank of DRAM memory, including a mode control input for

4   controlling the mode of said at least one bank of DRAM memory between a first mode and a

5   second mode, wherein when said at least one bank of DRAM memory is in said first mode, said

6   at least one bank of DRAM memory acts as physical memory, and when said at least one bank of

7   DRAM memory is in said second mode, said at least one bank of DRAM memory acts as cache

8   memory;

9   wherein the processing core and the at least one bank of DRAM memory are

10   fabricated on a single processor chip.

1   2.   (Original) The processor chip as recited in claim 1, wherein said processor chip is a first

2   processor chip which further comprises:

3   an I/O link configured to communicate with other processor chips; and

4   a communication and memory controller in electrical communication with said

5   processing core, said at least one bank of memory, and said I/O link;

6   said communication and memory controller for controlling the exchange of data

7   between said first processor chip and said other processor chips, and for receiving memory

8   requests from said processing core on said first processor chip and from other processing cores

9   on said other processor chips via said I/O link, and processing said memory requests with said at

10   least one bank of memory.

1   3.   (Original) The processor chip as recited in claim 2, wherein said communication and

2   memory controller comprises:

3   a first memory controller in electrical communication with said processing core

4   and said at least one bank of memory; and

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5   a second memory controller in electrical communication with said first memory

6   controller and said I/O link;

7   said second memory controller for controlling the exchange of data between said

8   first processor chip and said other processor chips;

9   said first memory controller for receiving memory requests from said processing

10 core on said first processor chip and said second memory controller, and process said memory

11 requests with said at least one bank of memory.

1   4.   (Original) The processor chip as recited in claim 2, wherein when said at least one bank

2   of memory on said first processor chip and said at least one bank of memory on said other

3   processor chips comprise physical memory, the data stored on said at least one bank of memory

4   on said first processor chip is different from the data stored on said at least one bank of memory

5   on said other processor chips.

1   5.   (Currently Amended) The processor chip as recited in claim 2, further comprising an

2   external memory interface in electrical communication with said communication and memory

3   controller;

4   said external memory interface for connecting said first processor chip in

5   electrical communication with external memory; and

6   said communication and memory controller for receiving memory requests from

7   said processing core on said first processor chip and from processing cores on said other

8   processor chips, determining whether said memory requests are directed to said at least on one

9   bank of memory on said first processor chip, to said at least one bank or memory on said other

10 processor chips, or to said external memory, and processing said memory requests with said at

11 least one bank of memory on said first processor chip, with said at least one bank of memory on

12 said other processor chips through said I/O link, or with said external memory through said

13 external memory interface.

1   6.   (Original) The processor chip as recited in claim 5, wherein said external memory is

2   DRAM.

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1   7.   (Original) The processor chip as recited in claim 5, wherein when said at least one bank

2   of memory on said first processor chip and said at least one bank of memory on said other

3   processor chips comprise physical memory, the data stored on said at least one bank of memory

4   on said first processor chip is different from the data stored on said at least one bank of memory

5   on said other processor chips and said external memory.

1   8.   (Original) In a computer system, a scalable computer processing architecture,

2   comprising:

3   one or more processor chips, each comprising:

4   a processing core;

5   at least one bank of DRAM memory including a mode control input for

6   controlling the mode of said at least one bank of DRAM memory between a first mode and a

7   second mode, wherein when said at least one bank of DRAM memory is in said first mode, said

8   at least one bank of memory acts as physical memory, and when said at least one bank of DRAM

9   memory is in said second mode, said at least one bank of DRAM memory acts as cache memory;

10   an I/O link configured to communicate with other of said one or more processor

11   chips or with I/O devices;

12   a communication and memory controller in electrical communication with said

13   processing core, said at least one bank of memory, and said I/O link;

14   said communication and memory controller for controlling the exchange of data

15   between said one or more processor chips and I/O devices, and for receiving memory requests

16   from said processing cores on said one or more processor chips and from said I/O devices, and

17   processing said memory requests with said at least one bank of memory.

18   wherein said computer processing architecture can be scaled larger by connecting

19   together two or more of said processor chips in parallel via said I/O links of said processor chips,

20   so as to create multiple processing core pipelines which share data therebetween.

1   9.   (Original) The processor chip as recited in claim 8, wherein said communication and

2   memory controller on said one or more processor chips comprises:

3   a first memory controller in electrical communication with said processing core

4   and said at least one bank of memory; and

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5   a second memory controller in electrical communication with said first memory

6 controller and said I/O link;

7   said second memory controller for controlling the exchange of data between said

8 processor chip and said other processor chips;

9   said first memory controller for receiving memory requests from said processing

10 core and said second memory controller, and process said memory requests with said at least one

11 bank of memory.

1 10.   (Original) The processor chip as recited in claim 8, wherein when said at least one bank

2 of memory on said one or more processor chips comprise physical memory, the data stored on

3 said at least one bank of memory on each of said one or more processor chips is different from

4 the data stored on said at least one bank of memory on each of the other of said one or more

5 processor chips.

1 11.   (Original) The computer processing architecture as recited in claim 8, wherein at least

2 one of said one or more processor chips further comprises an external memory interface in

3 electrical communication with said communication and memory controller;

4   said external memory interface for connecting said at least one of said one or

5 more processor chips in electrical communication with external memory; and

6   said communication and memory controller of said at least one of said one or

7 more processor chips for receiving memory requests from said processing cores of said one or

8 more processor chips and said I/O devices, determining whether said memory requests are

9 directed to said at least one bank of memory on said at least one of said one or more processor

10 chips, to other of said one or more processor chips, or to said external memory, and processing

11 said memory requests with said at least one bank of memory on said at least one of said one or

12 more processor chips, with said other of said one or more processor chips, or with said external

13 memory through said external memory interface.

1 12.   (Original) The computer processing architecture as recited in claim 11, wherein said

2 external memory comprises DRAM.

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1   13.   (Original) The processor chip as recited in claim 11, wherein when said at least one bank

2   of memory on said one or more processor chips comprise physical memory, the data stored on

3   said at least one bank of memory on each of said one or more processor chips is different from

4   the data stored on said at least one bank of memory on each of the other of said one or more

5   processor chips and said external memory.

1   14.   (Original) The computer processing architecture as recited in claim 8, comprising a first

2   and a second processor chip, wherein said processing core on said first processor chip is

3   configured to access said at least one bank of memory on said second processor chip through the

4   I/O links of said first and said second processor chips.

1   15.   (Original) The computer processing architecture as recited in claim 14, wherein a

2   memory request directed from said processing core on said first processor chip to said at least

3   one bank of memory on said second processor chip is processed by:

4   said processing core on said first processor chip sending a memory request to said

5   communication and memory controller on said first processor chip;

6   said communication and memory controller on said first processor chip

7   determining that said memory request is not accessing said at least one bank of memory on said

8   first processor chip, and passing said memory request to said communication and memory

9   controller on said second processor chip via said I/O links on said first and said second processor

10   chips;

11   said communication and memory controller on said second processor chip

12   processing said memory request with said at least one bank of memory on said second processor

13   chip by performing a memory access function with said at least one bank of memory on said

14   second processor chip;

15   said communication and memory controller on said second processor chip passing

16   a result of said memory access function back to said communication and memory controller on

17   said first processor chip via said I/O links on said first and said second processor chips; and

18   said communication and memory controller on said first processor chip

19   communicating said result of said memory access function to said processing core on said first

20   processor chip.

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1   16.   (Original) In a computer architecture having a plurality of processor chips, each

2   comprising a processing core and at least one bank of memory, a method for a first processing

3   core on a first processor chip of accessing said at least one bank of memory on a second

4   processor chip, comprising the steps of:

5   said first processing core on said first processor chip issuing a memory request;

6   determining whether said memory request is accessing data in said at least one

7   bank of memory on said first processor chip or data in said at least one bank of memory on said

8   second processor chip;

9   if said memory request is accessing data in said at least one bank of memory on

10   said second processor chip, communicating said memory request to said second processor chip;

11   performing a memory access function to said at least one bank of memory on said

12   second processor chip; and

13   communicating a result of said memory access function back to said first

14   processing chip.

1   17.   (Original) The method as recited in claim 16, wherein said at least one bank or memory

2   on each of said plurality of processing chips comprises physical memory.

1   18.   (Original) The method as recited in claim 16, wherein said at least one bank of memory

2   on each of said plurality of processing chips comprises cache memory.

1   19.   (Original) The method as recited in claim 16, wherein said at least one bank of memory

2   on each of said plurality of processing chips further comprises a mode control input, and wherein

3   said at least one bank of memory on each of said plurality of processing chips can switch

4   between physical memory and cache memory by enabling or disabling said mode control input.